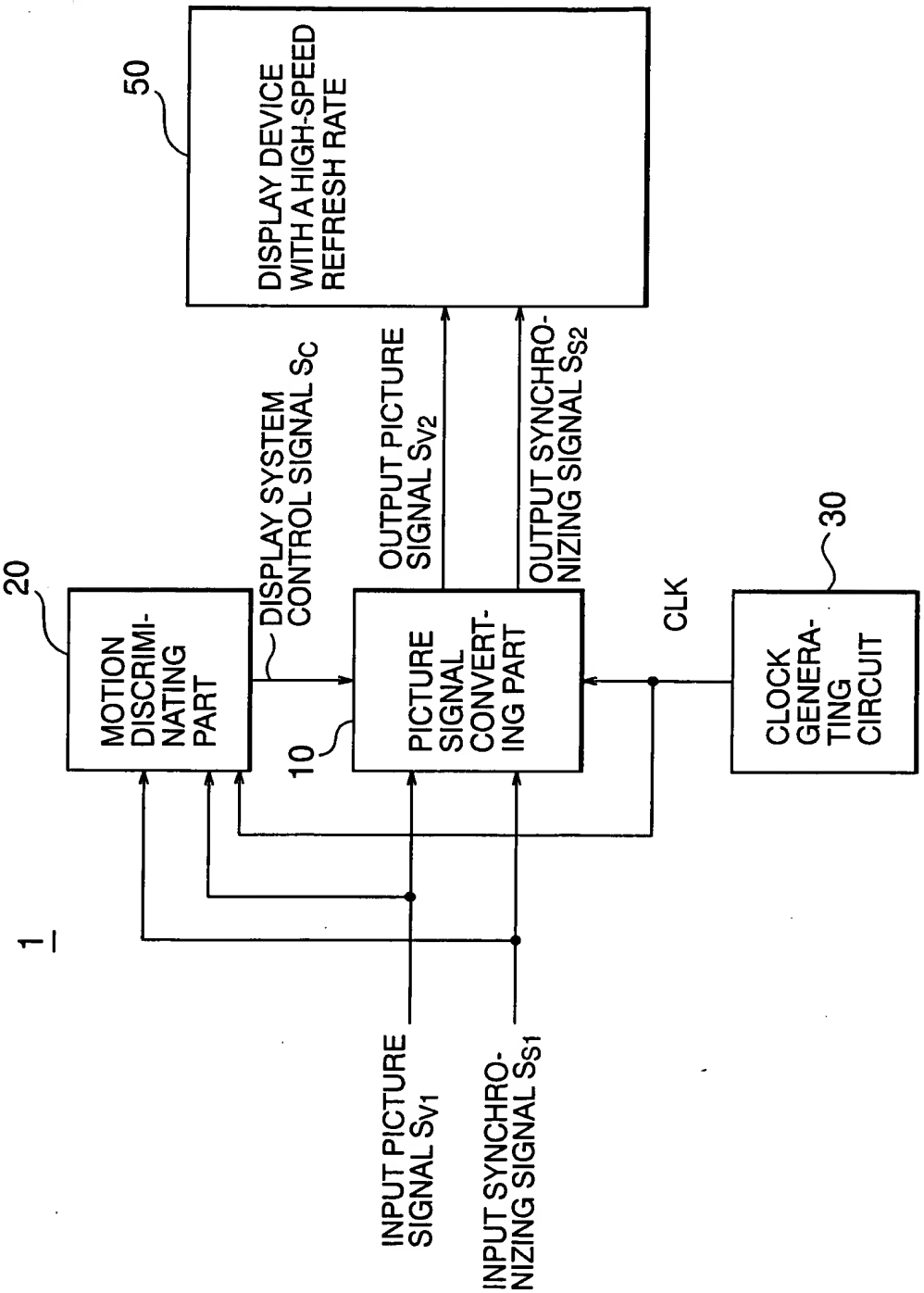


FIG. 1

TOP90 "08150860

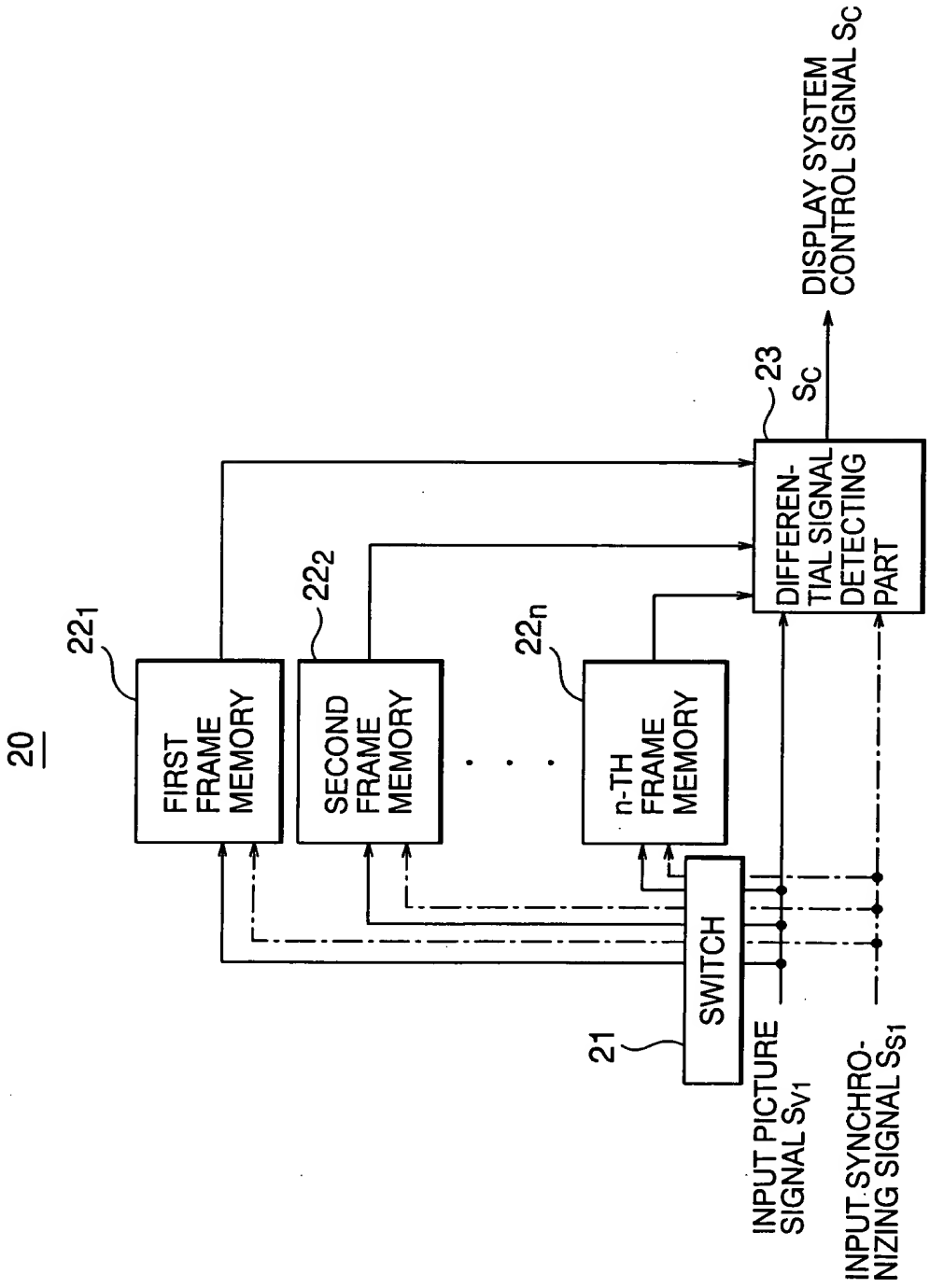


FIG. 2

TOP290 "BC15860

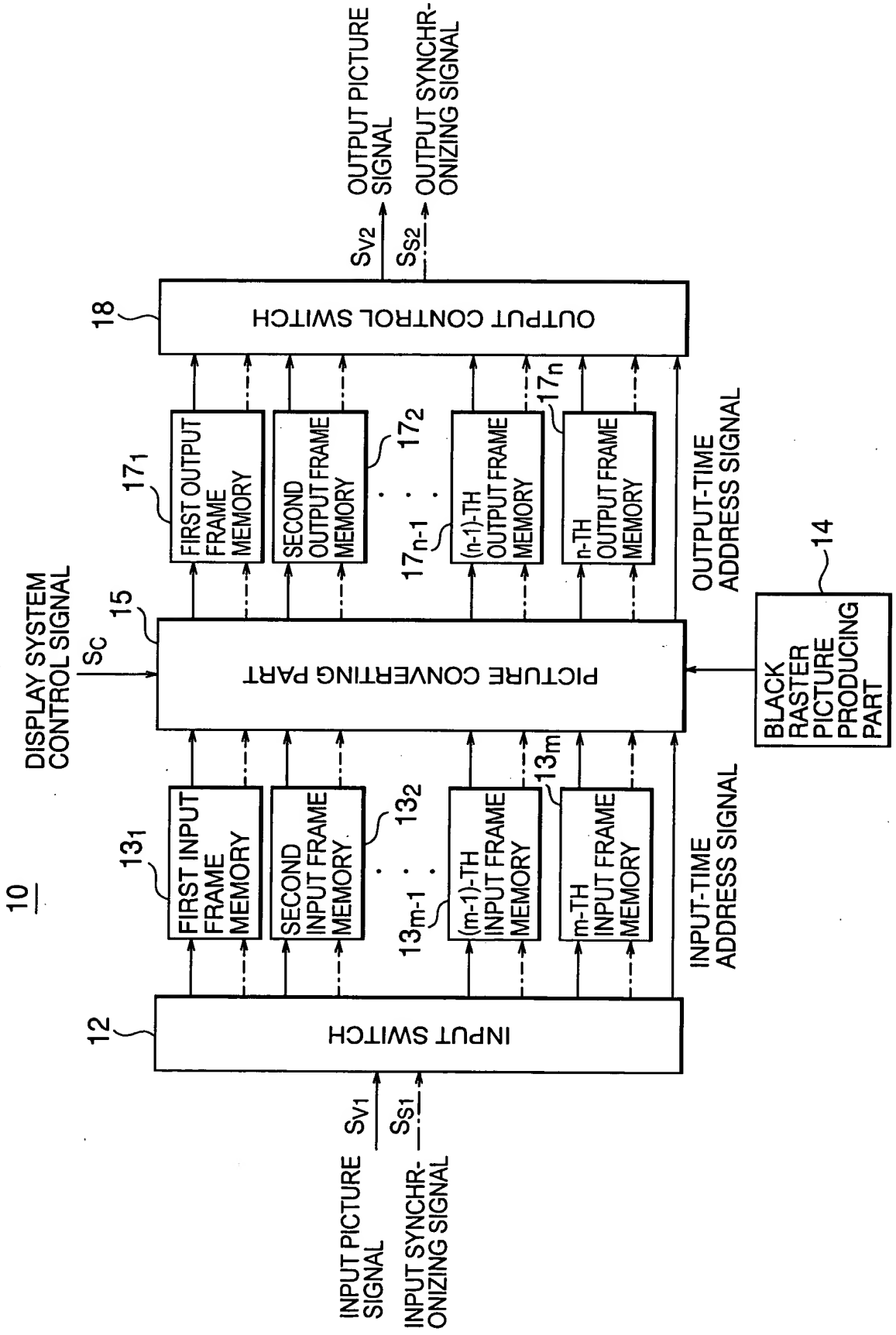

10
INPUT PICTURE SIGNAL
INPUT SYNCHRONIZING SIGNAL
S_{V1}
S_{S1}
12
INPUT SWITCH
13_1
FIRST INPUT FRAME MEMORY
SECOND INPUT FRAME MEMORY
13_2
13_{m-1}
(m-1)-TH INPUT FRAME MEMORY
13_m
m-TH INPUT FRAME MEMORY
INPUT-TIME ADDRESS SIGNAL
DISPLAY SYSTEM CONTROL SIGNAL
S_C
15
PICTURE CONVERTING PART
14
BLACK RASTER PICTURE PRODUCING PART
OUTPUT-TIME ADDRESS SIGNAL
17_1
FIRST OUTPUT FRAME MEMORY
SECOND OUTPUT FRAME MEMORY
17_2
17_{n-1}
(n-1)-TH OUTPUT FRAME MEMORY
17_n
n-TH OUTPUT FRAME MEMORY
18
OUTPUT CONTROL SWITCH
S_{V2}
S_{S2}
OUTPUT PICTURE SIGNAL
OUTPUT SYNCHRONIZING SIGNAL

FIG. 3

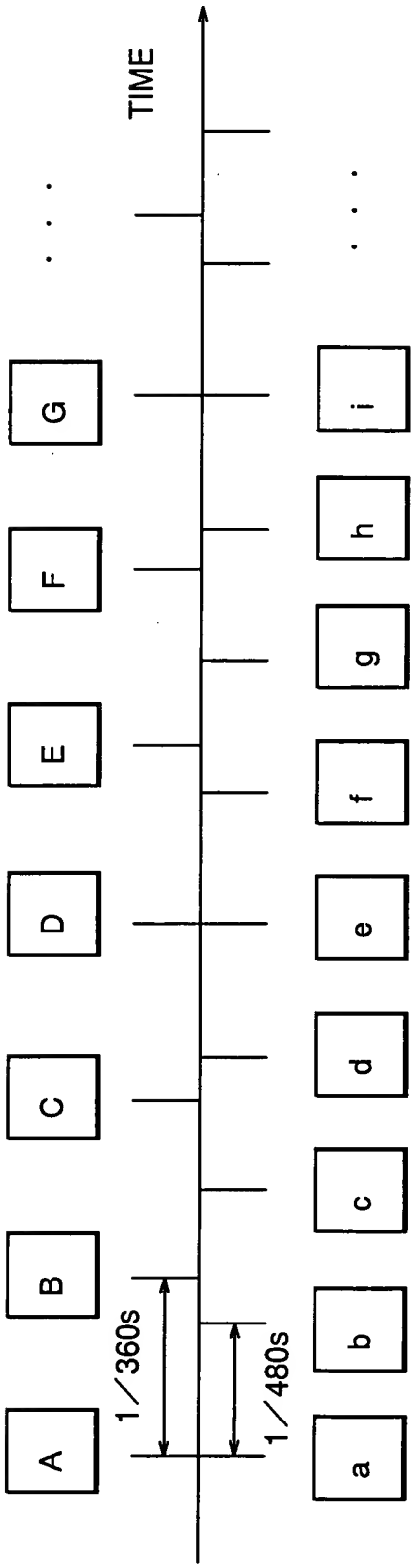


FIG. 4

EOL250: 8E15880

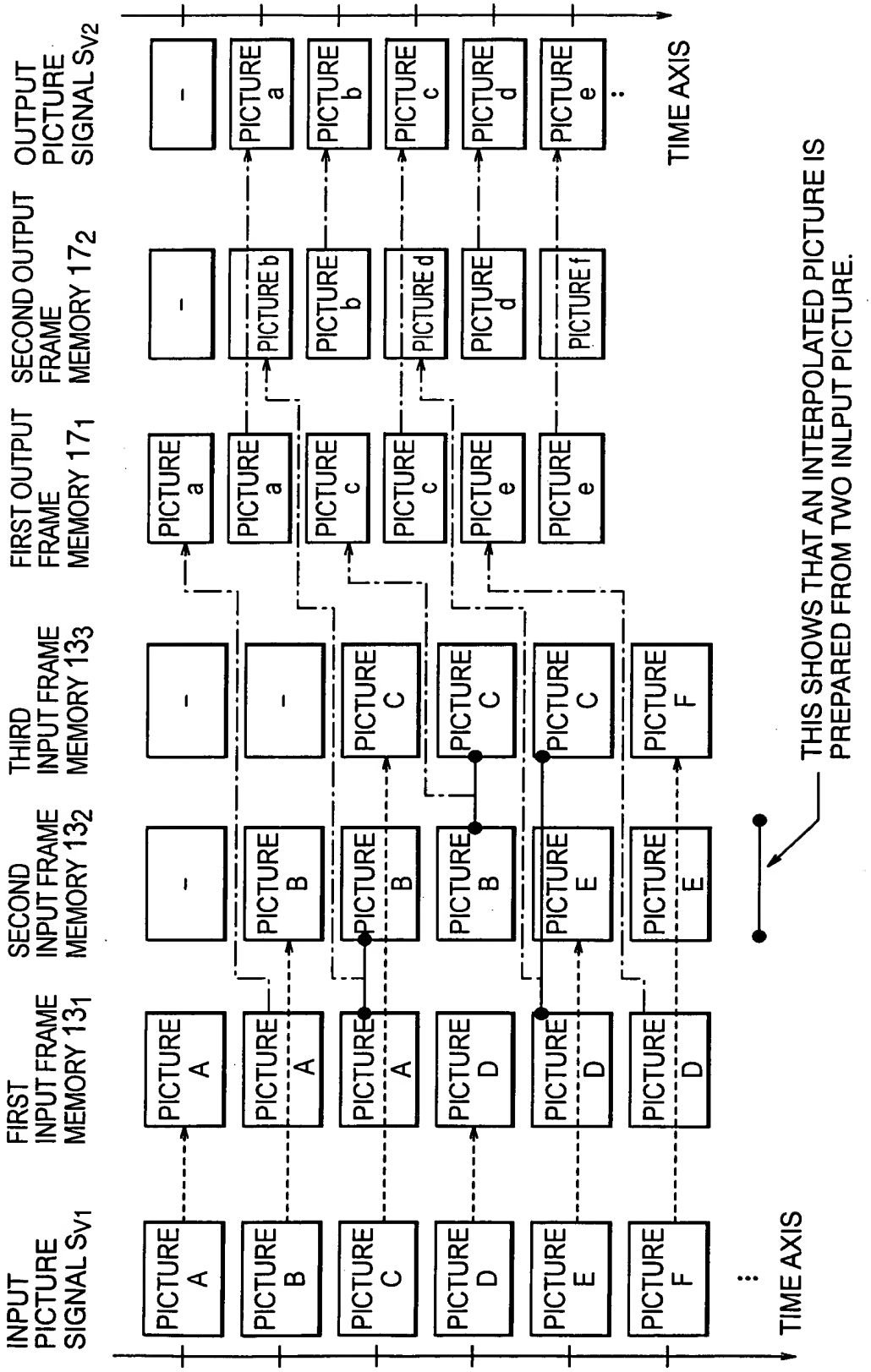

INPUT PICTURE SIGNAL S_{V1}
FIRST INPUT FRAME MEMORY 13_1
SECOND INPUT FRAME MEMORY 13_2
THIRD INPUT FRAME MEMORY 13_3
FIRST OUTPUT FRAME MEMORY 17_1
SECOND OUTPUT FRAME MEMORY 17_2
OUTPUT PICTURE SIGNAL S_{V2}
ADDRESS
ADDRESS
TIME AXIS
TIME AXIS
PICTURE A
PICTURE B
PICTURE C
PICTURE D
PICTURE E
PICTURE F
PICTURE a
PICTURE b
PICTURE c
PICTURE d
PICTURE e
PICTURE f
THIS SHOWS THAT AN INTERPOLATED PICTURE IS PREPARED FROM TWO INLPUT PICTURE.

FIG. 5

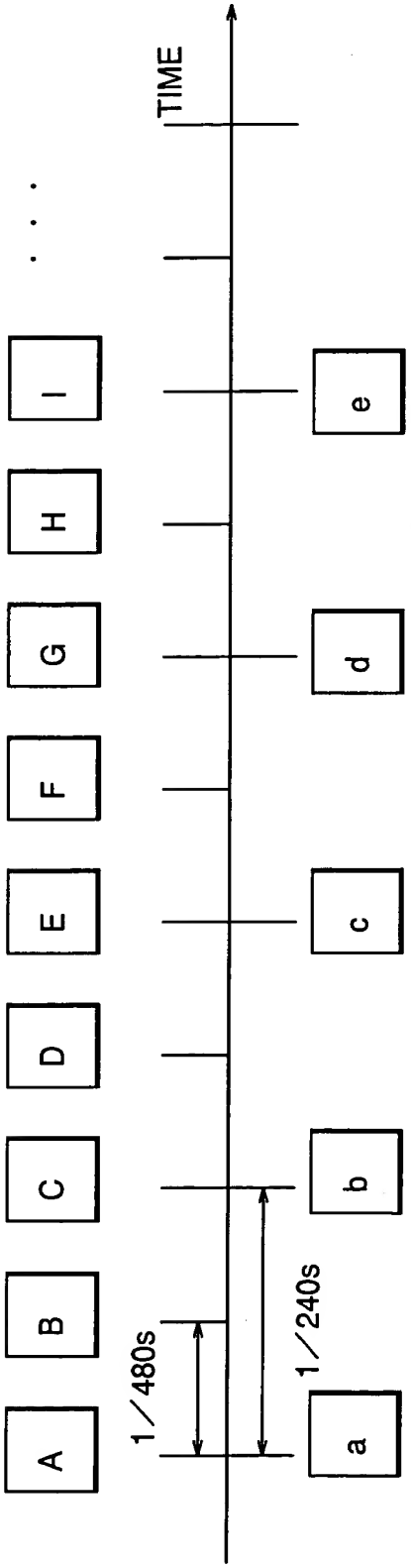


FIG. 6

TOP290 "85T58850

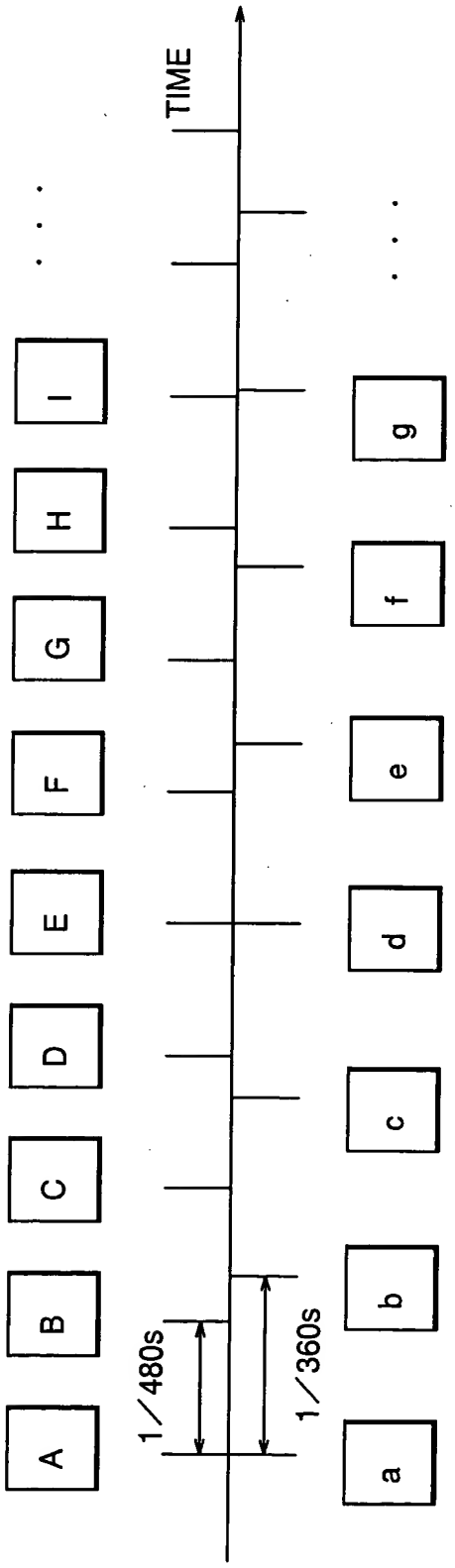


FIG. 7

EP 2 750 394 A1

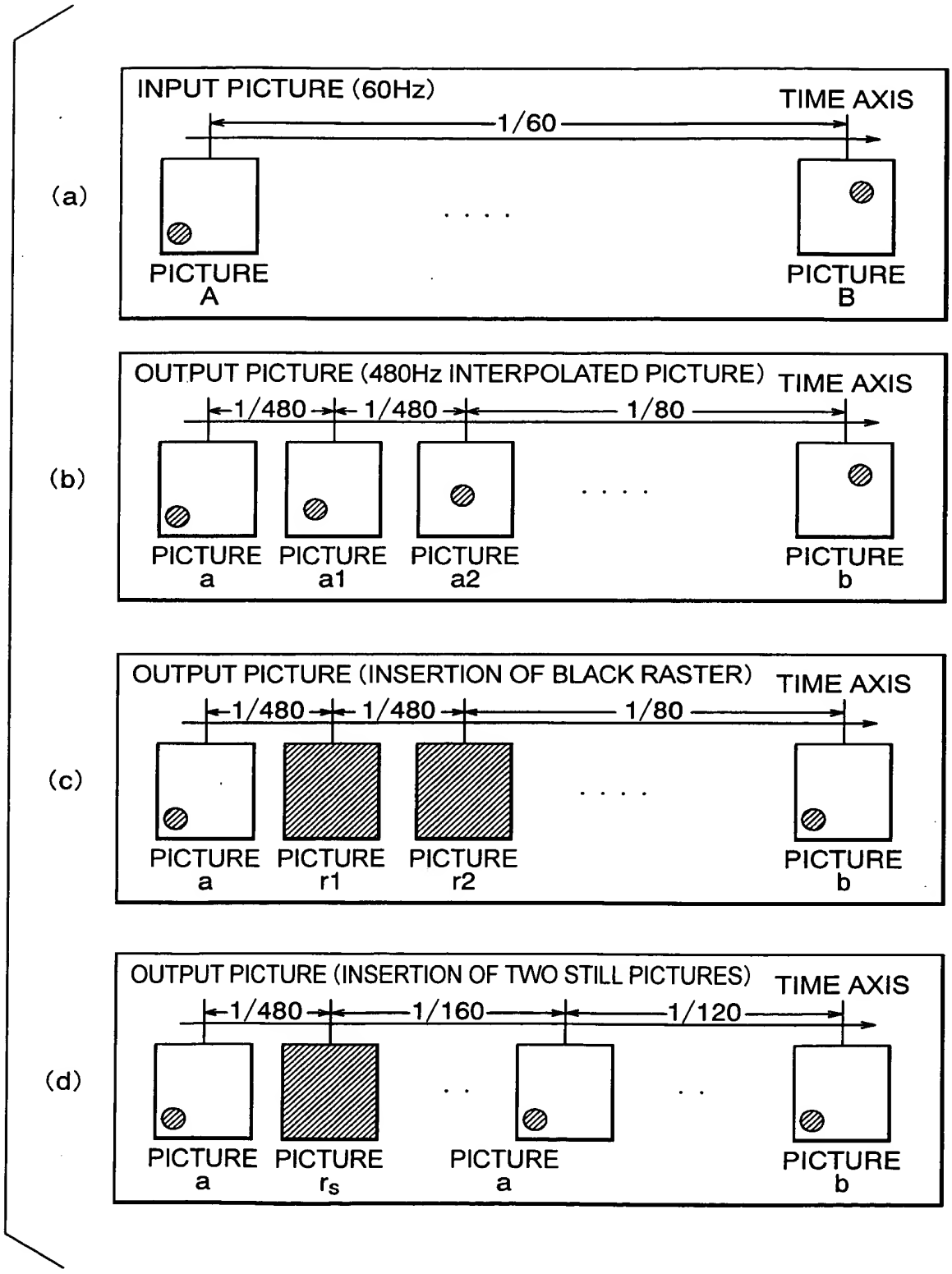


FIG. 8

EP 0 762 748 A2

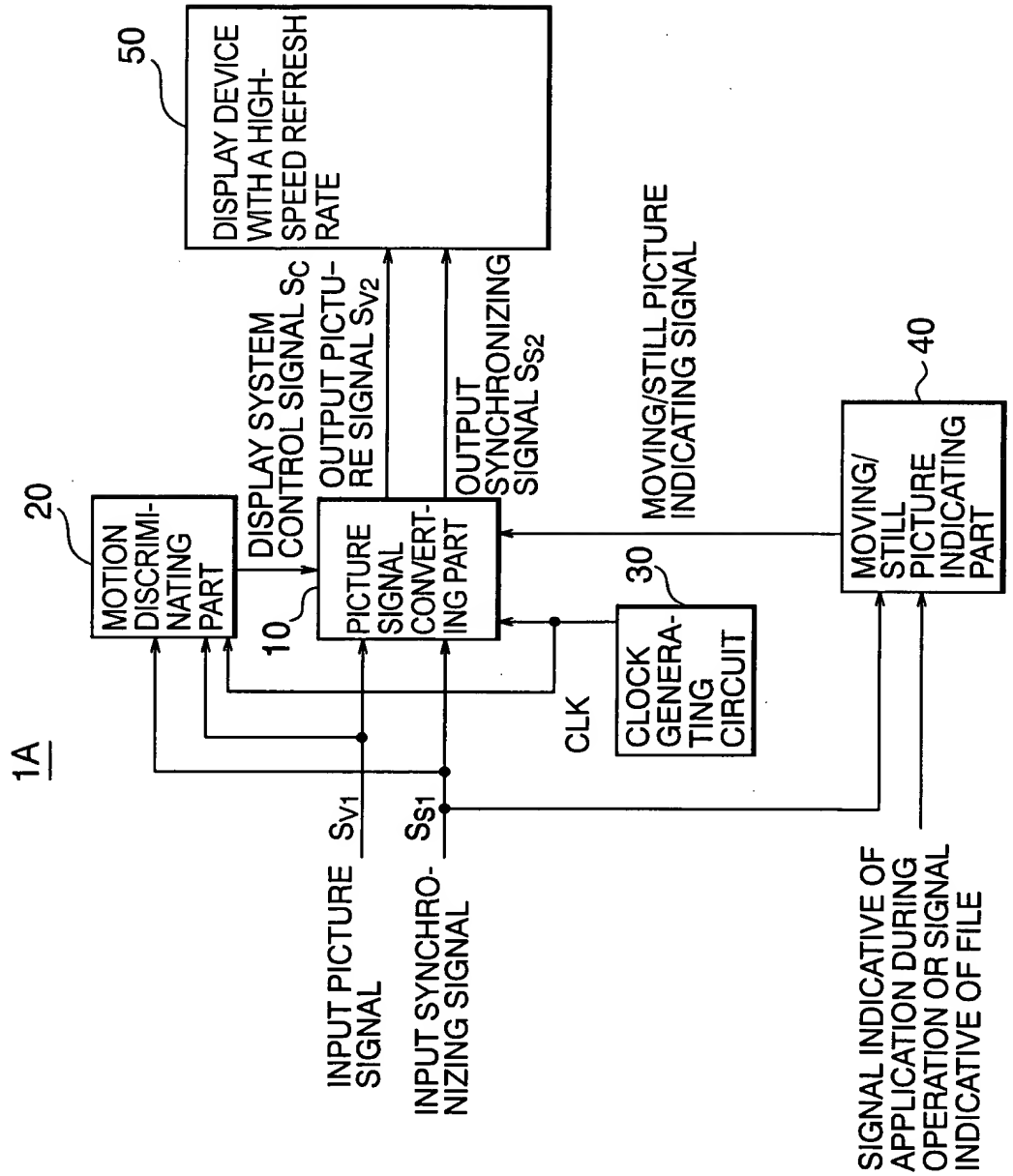

1A
20
MOTION DISCRIMI-NATING PART
10
PICTURE SIGNAL CONVERT-ING PART
30
CLOCK GENERA-TING CIRCUIT
CLK
40
MOVING/ STILL PICTURE INDICATING PART
50
DISPLAY DEVICE WITH A HIGH-SPEED REFRESH RATE
DISPLAY SYSTEM CONTROL SIGNAL Sc
OUTPUT PICTU-RE SIGNAL Sv2
OUTPUT SYNCHRONIZING SIGNAL Ss2
MOVING/STILL PICTURE INDICATING SIGNAL
INPUT PICTURE SIGNAL Sv1
INPUT SYNCHRO-NIZING SIGNAL Ss1
SIGNAL INDICATIVE OF APPLICATION DURING OPERATION OR SIGNAL INDICATIVE OF FILE

FIG. 9

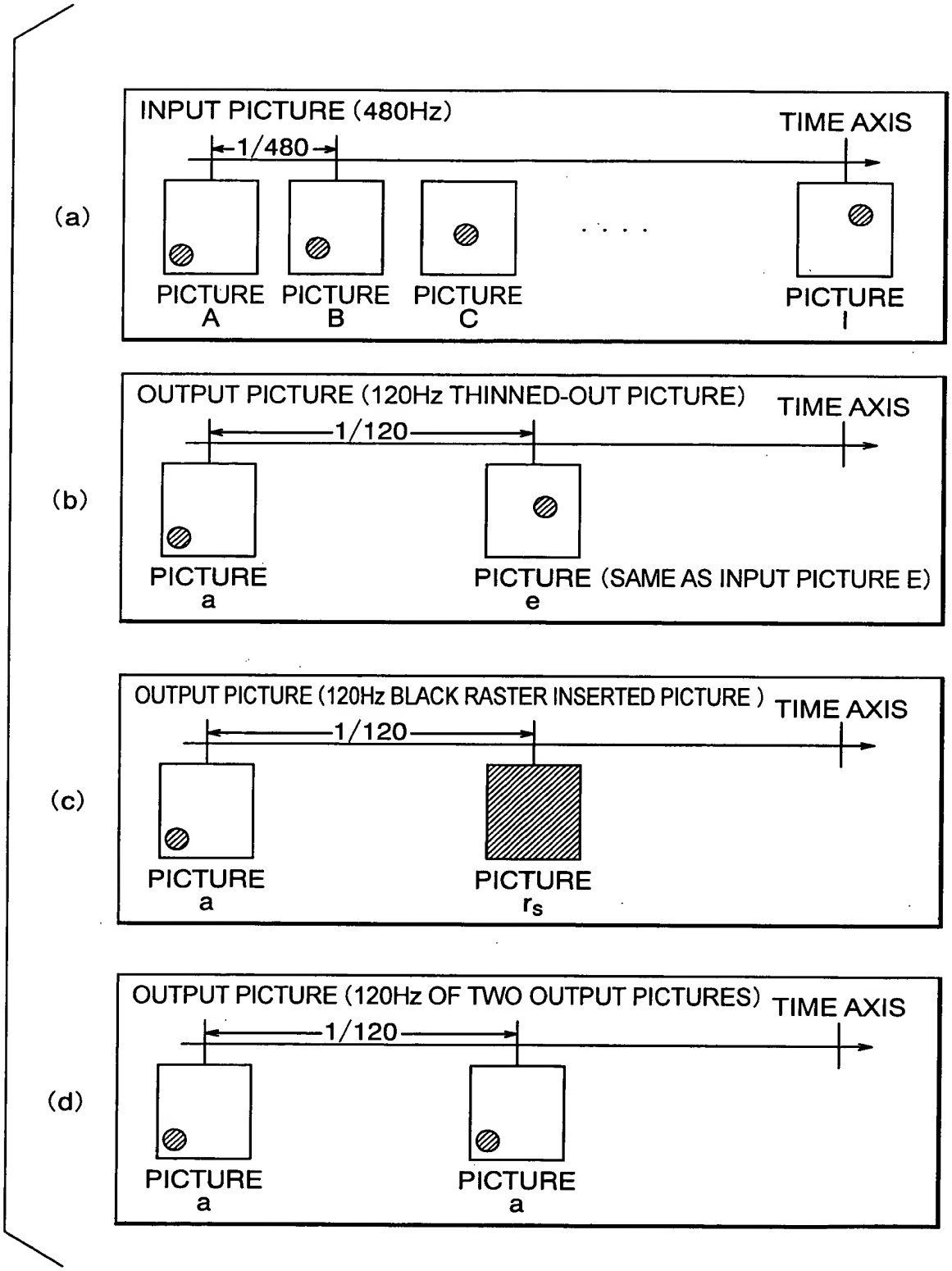


FIG. 10

EP 1 351 508 A2

1-0F2210:8E2E5660

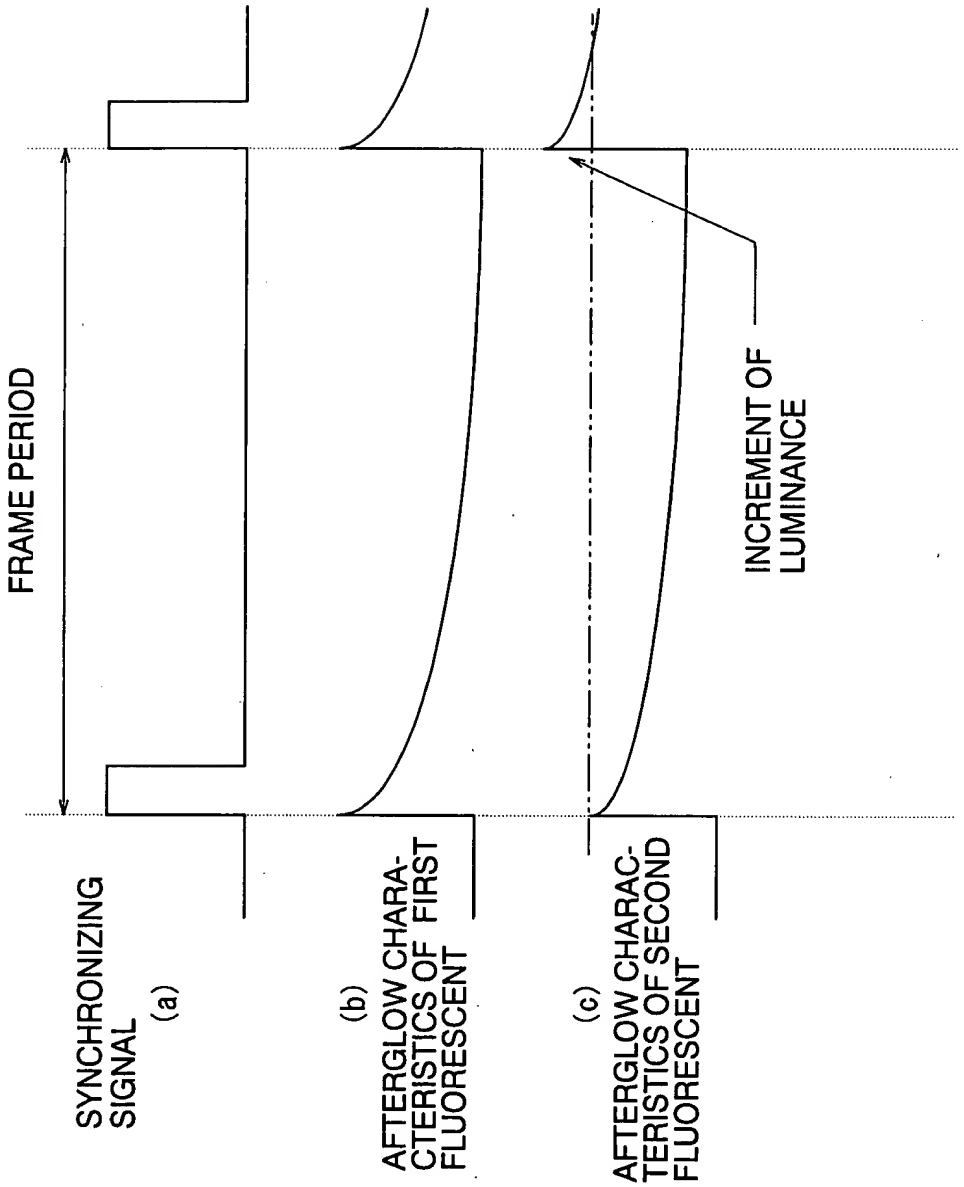


FIG. 11

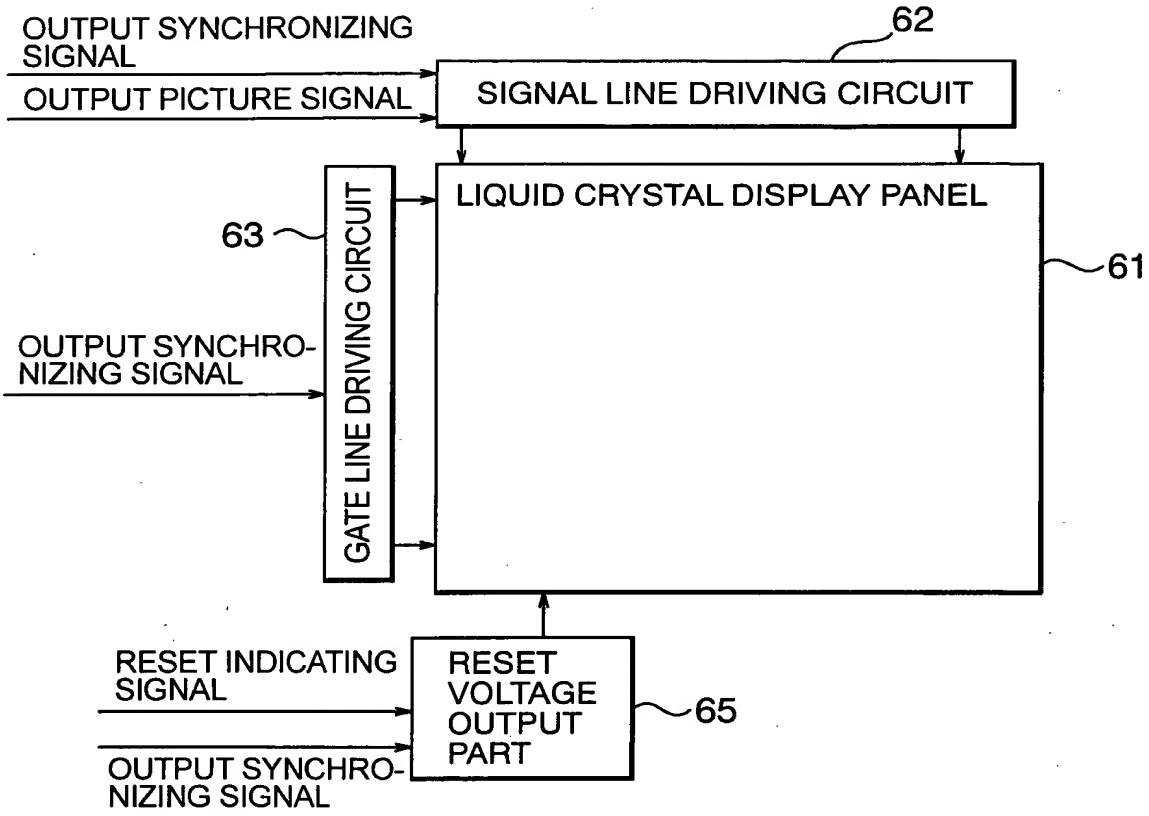
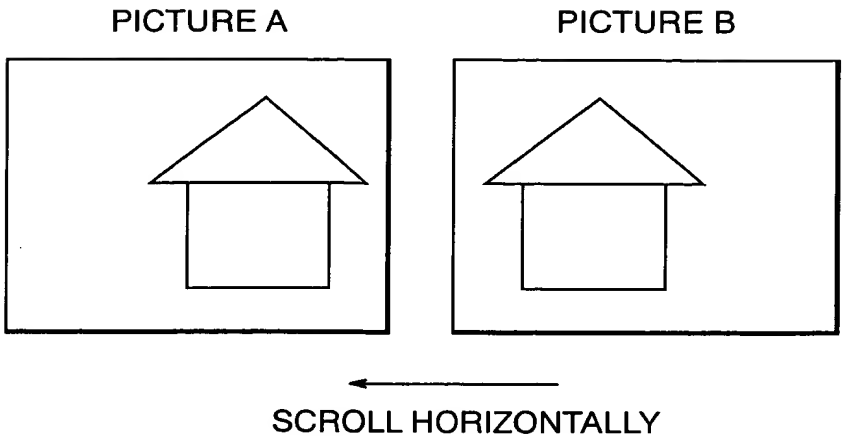


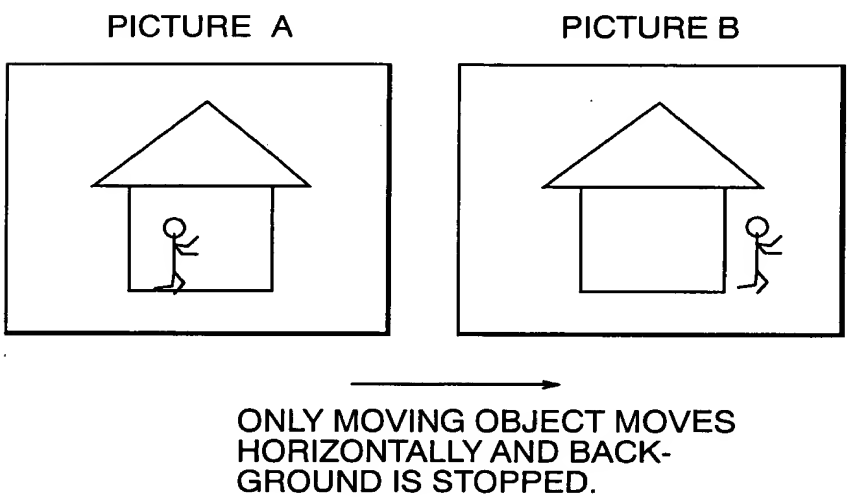
FIG. 12

EP 1 365 385 A2

(a)



(b)



(c)

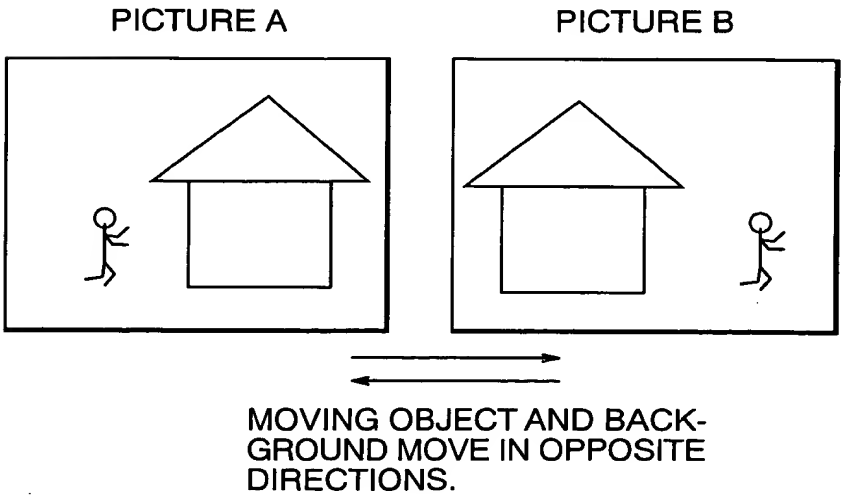


FIG. 13

Docket #210153US2RD

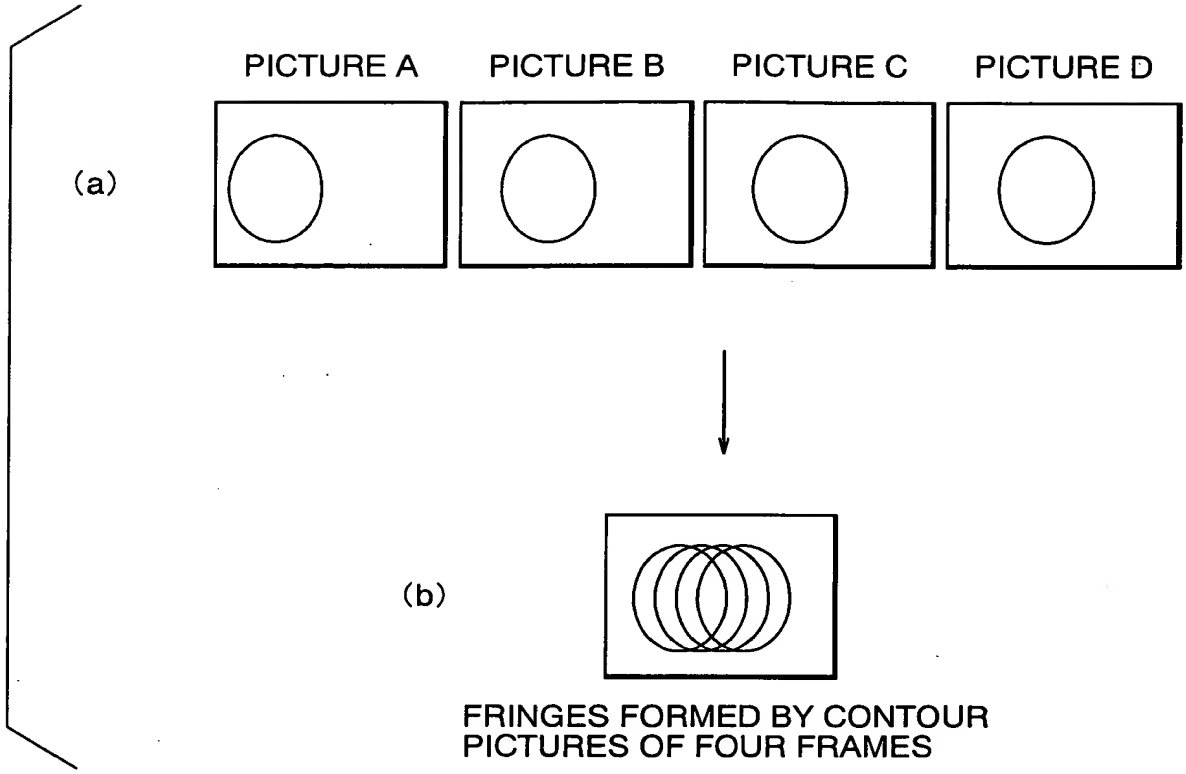


FIG. 14

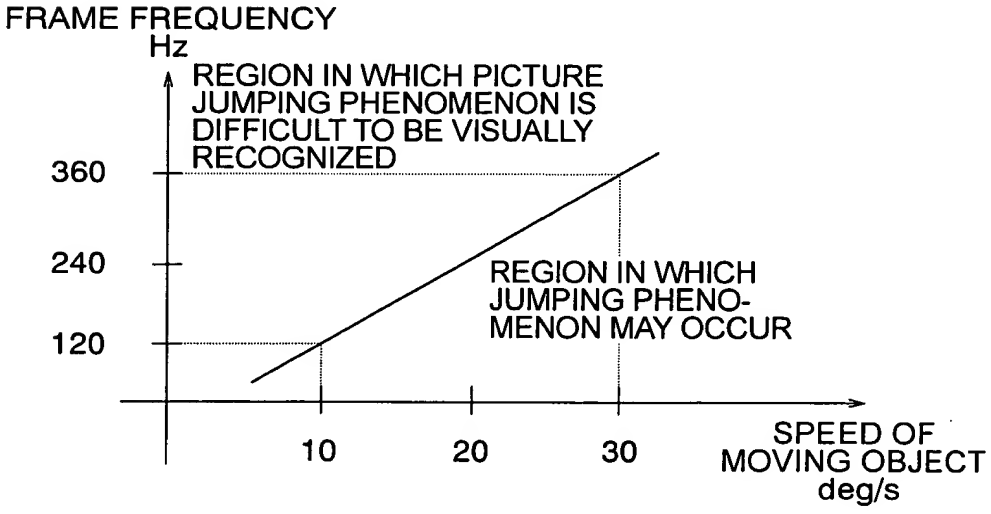


FIG. 15

EP 1 052 101 A2 20001115

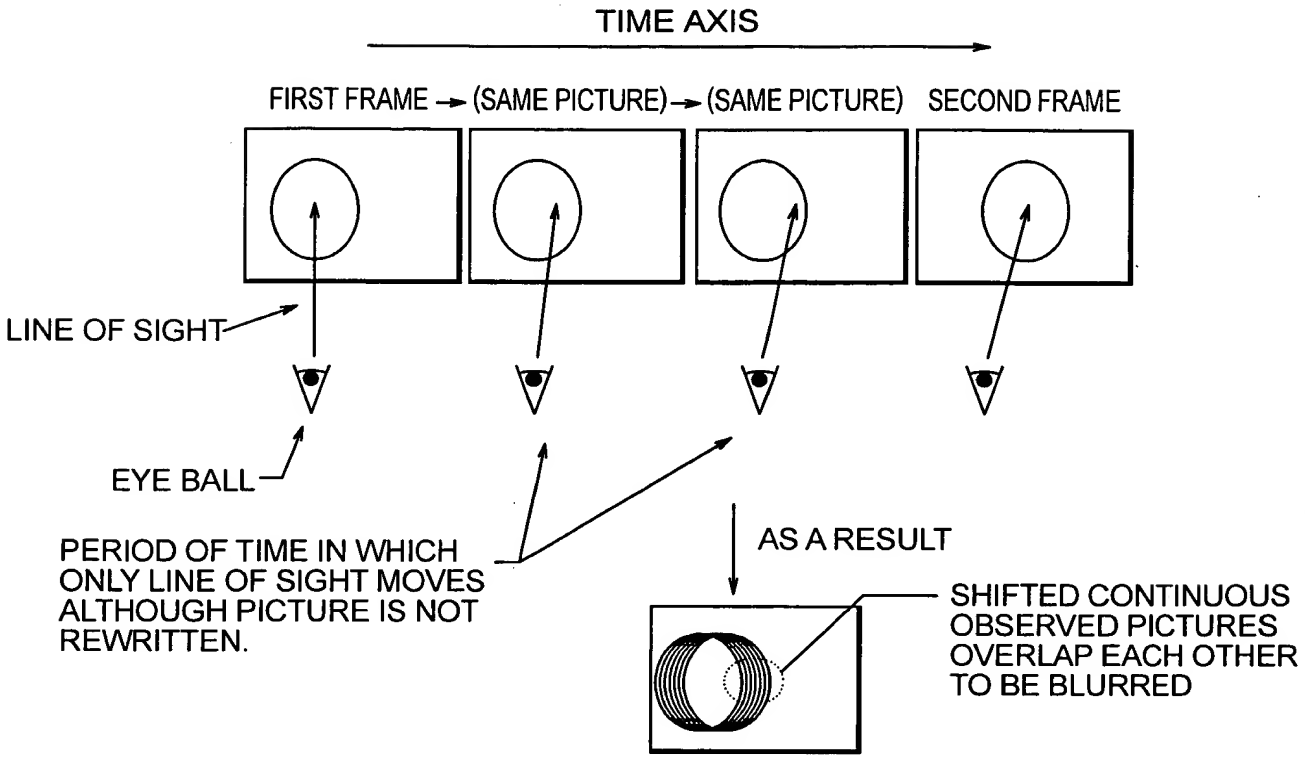


FIG. 16

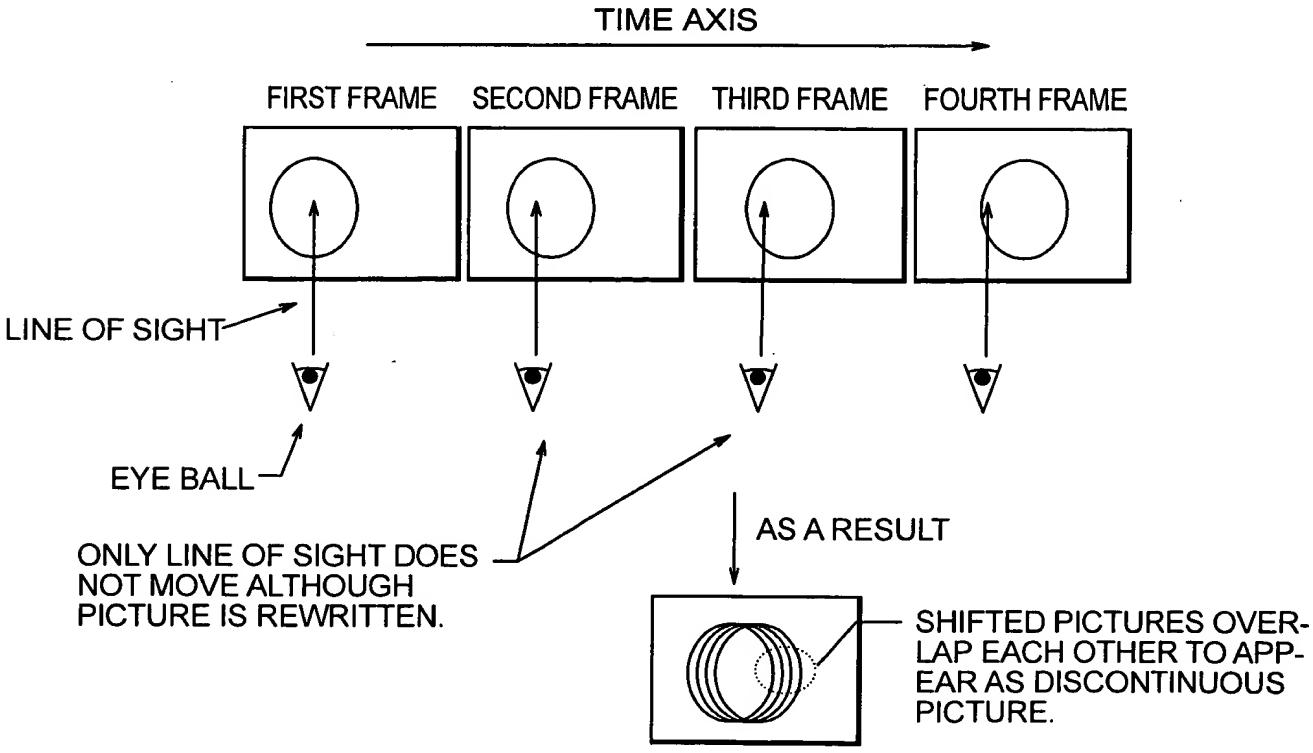


FIG. 17

09854388 - 062401

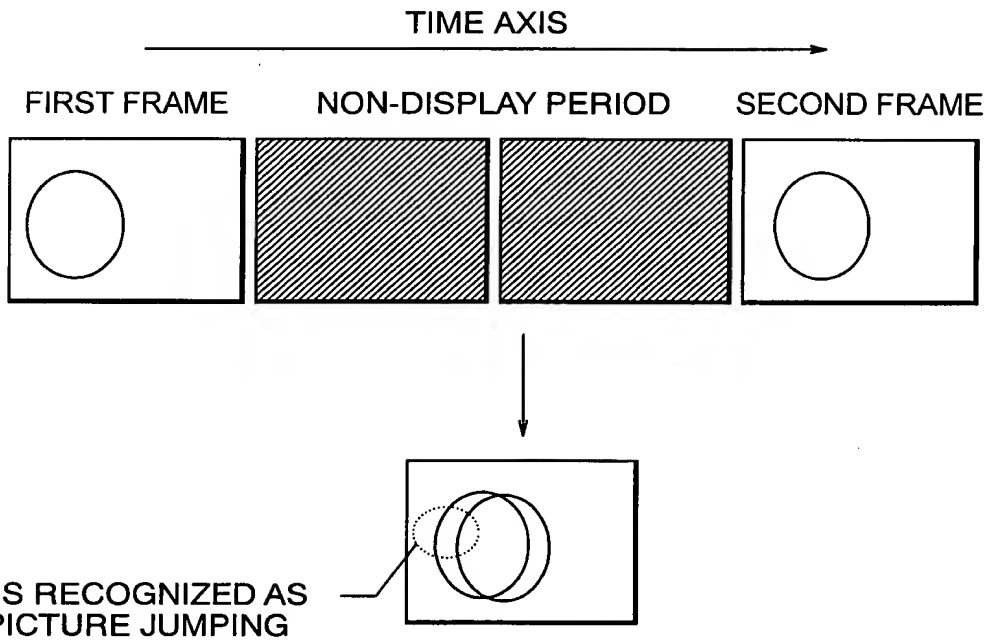


FIG. 18

EP 1 508 893 A2

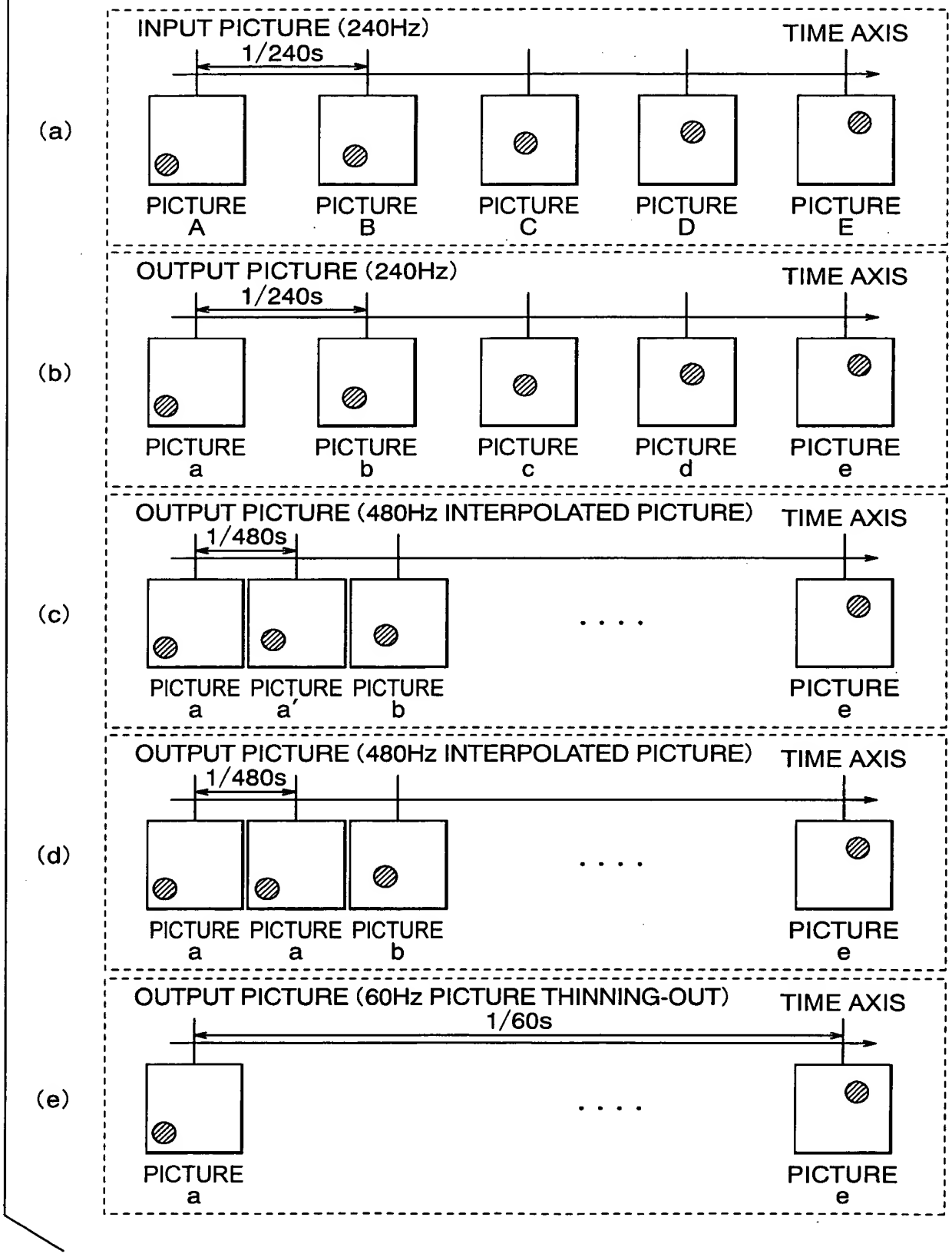


FIG. 19

EP 0 963 121 A1

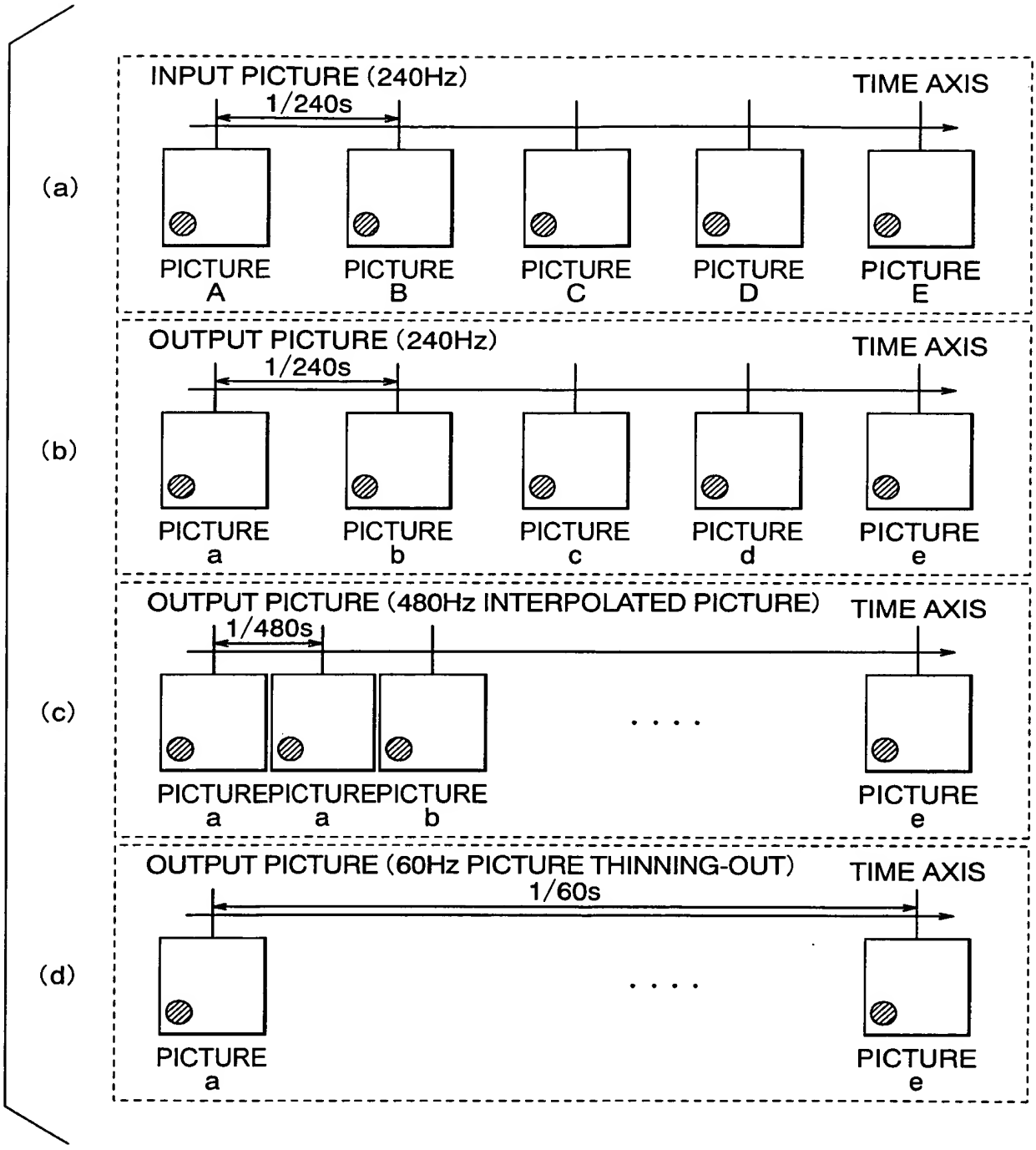


FIG. 20

EP 2 096 873 A1

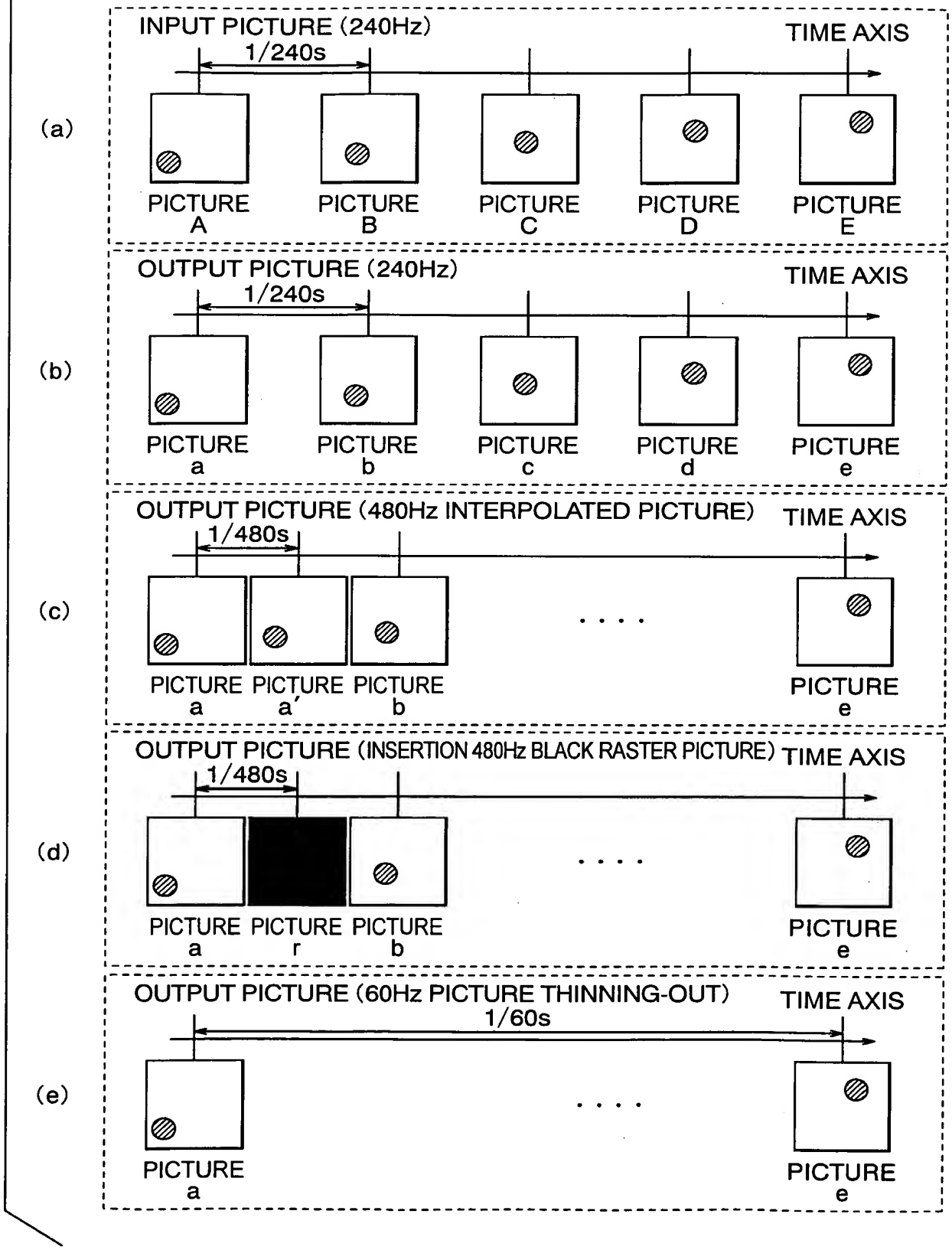


FIG. 21

EP 1 396 838 A2 20040310

EP 0 969 674 A1

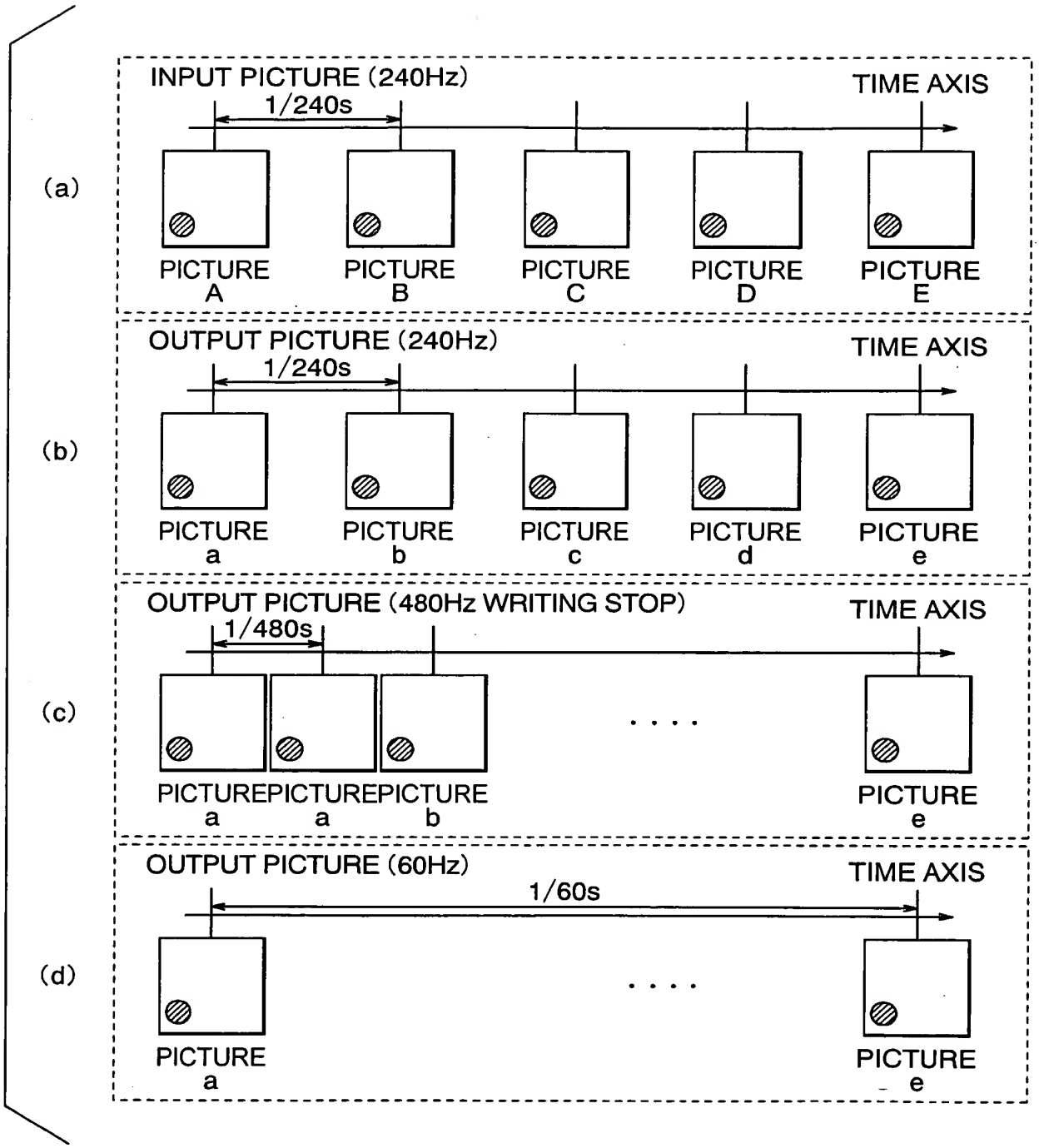


FIG. 22

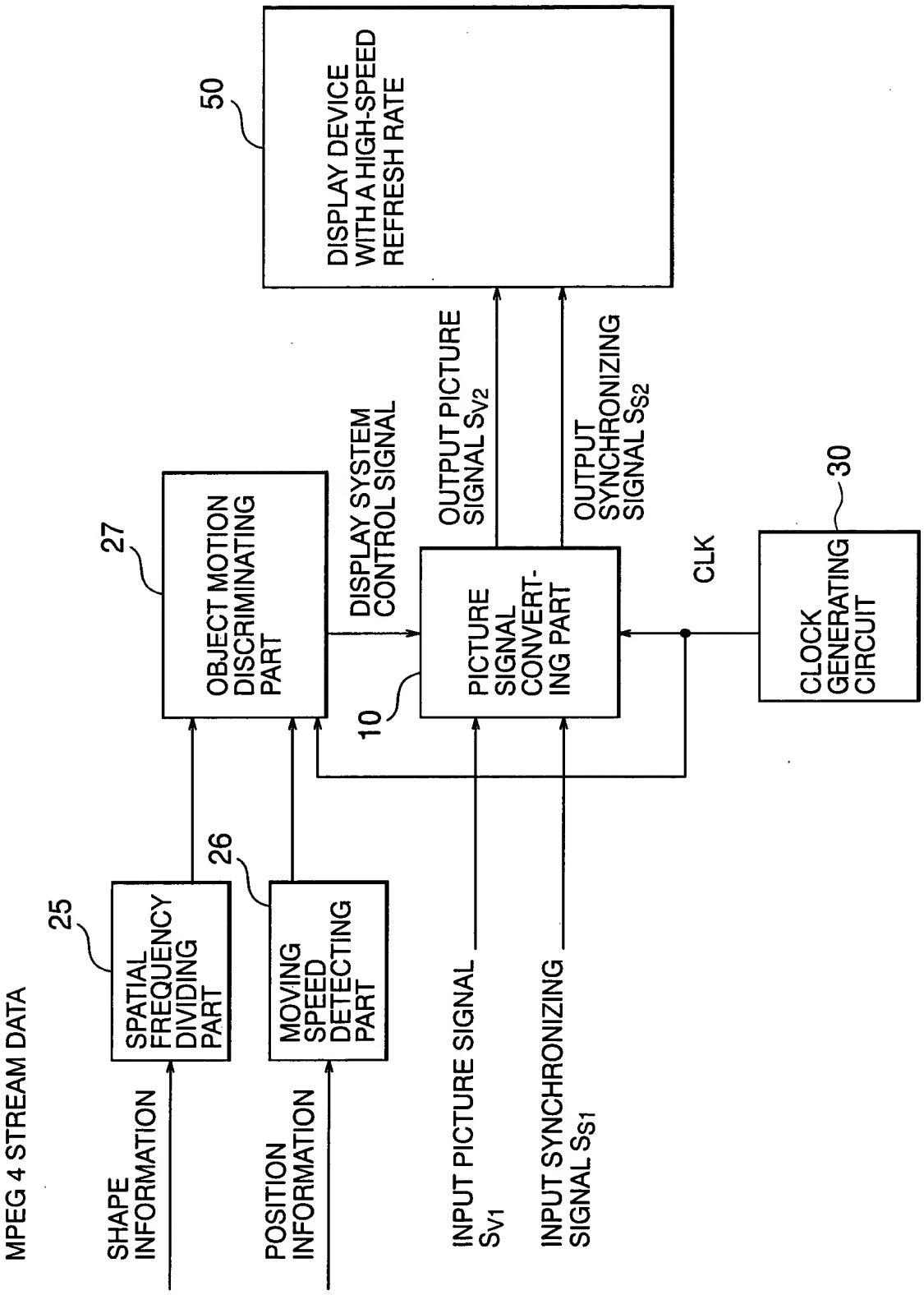

MPEG 4 STREAM DATA
SHAPE INFORMATION
POSITION INFORMATION
INPUT PICTURE SIGNAL S_{V1}
INPUT SYNCHRONIZING SIGNAL S_{S1}
25
SPATIAL FREQUENCY DIVIDING PART
26
MOVING SPEED DETECTING PART
27
OBJECT MOTION DISCRIMINATING PART
DISPLAY SYSTEM CONTROL SIGNAL
10
PICTURE SIGNAL CONVERT-ING PART
OUTPUT PICTURE SIGNAL S_{V2}
OUTPUT SYNCHRONIZING SIGNAL S_{S2}
CLK
30
CLOCK GENERATING CIRCUIT
50
DISPLAY DEVICE WITH A HIGH-SPEED REFRESH RATE

FIG. 23